REMARKS

Following entry of this Amendment, claims 1, 3-7, 10, 11, 13-19 and 100-111 are pending in the above-identified application. Claims 1, 3-7, 10, 11, 13-19 are rejected under 35 U.S.C. §102(b) as being anticipated by Barrio ("Study of the Techniques for Emulation Programming"). Claims 2, 8, 9, 12 and 20-99 have been canceled to facilitate prosecution of this application. Each of new claims 100-111 are either an apparatus (claims 100-105) or programming products (claims 106-111) that corresponds to one of the existing method claims 1, 3-7, 10, 11, 13-19. Elements not originally in the method claims are a "processor," which is supported in the Specification at **FIGs. 1** and **2**, elements **12** and **22** and related description at **¶¶[0023]** and **[0030]**, and a "memory," which is supported in **FIG. 1**, element **18** and corresponding description at **¶[0023]**.

In the Response to Arguments for the current Final Office Action, dated February 5, 2009, (FOA), the Examiner states:

Regarding the Applicant's amendment for the rejection addressed under 35 USC 112 second paragraph, Applicant fail [*sic*] to clarify the "subject code". To expidite the action, this rejection will be withdrawn, but the recitation "a subject code" will be interpreted as the target code that is translated by an emulator for a target processor (p. 2, lines 9-12).

Applicants submit that these amendments and remarks overcome all of the Examiner's outstanding objections and rejections and bring the present Application into condition for allowance. Entry of this amendment and a notice of allowance of all the remaining claims are therefore respectfully solicited.

Rejections Based on §112 ¶2

Applicants appreciate the withdrawal of the §112 ¶2 rejections in the previous Office Action. In the Response to Arguments for the current Final Office Action, dated February 5, 2009, (FOA), the Examiner states:

> Regarding the Applicant's amendment for the rejection addressed under 35 USC 112 second paragraph, Applicant fail [*sic*] to clarify the

> "subject code". To expedite the action, this rejection will be withdrawn, but the recitation "a subject code" will be interpreted as the target code that is translated by an emulator for a target processor

(p. 2, lines 9-12). The Applicants submit that the interpretation above unnecessarily mixes the concepts of "subject code" and "target code." Simply stated, subject code is code prior to processing by an emulator and target code is code after processing by an emulator. One example of this is clearly illustrated in elements **10**, **20** and **30** of Applicants' **FIG. 2** and the corresponding description at **¶¶[0028]-[0031]**.

Rejections Based on §102(e)

Claims 1, 3-7, 10, 11, 13-19 are rejected under 35 U.S.C. §102(b) as being anticipated by Barrio. Simply stated, Barrio is not executing a block of subject code through an emulator, executing the same block natively and then comparing the results. The current Office Action, dated February 5, 2009, (FOA) relies upon a Barris' description of an interpreter to suggest "executing a block of subject code." Barrio states:

> The CPU must decode these bytes and decide what it has to do. Then it performs the action commanded, updates de [*sic*] PC counter and reads another byte or bytes... [I]t read a byte (or the number of bytes which form an instruction in the emulated CPU). Then it decides which operation must be performed, and at last it executes the functions which [*sic*] correspond to that instruction.

(p. 18, lines 10-14). In other words, Barris describes executing not blocks of code but rather instructions line-by-line. The blocks of code described correspond to the interpreter in which a case statement translates "OPCODE1" to "opcode1();" "OPCODE2" to "opcode2():" and so on. In this example, the interpreter is executing in blocks however the interpreted code is executed one instruction at a time.

Barris is also not comparing the results of execution of blocks of code. The cited portion states:

> [T]o properly test a CPU emulator it would mean to generate all possible instructions which can receive the CPU and compare the result in the emulator with the real result. It will also be necessary to test combinations of instructions ...

(p. 24, lines 31-24). Testing each instruction, or even "combinations of instructions," is not analogous to testing "blocks of code" because the phrase "blocks of code" is not merely "combinations of instructions." Barris does not describe testing actual code in the manner of the claimed subject matter.

With respect to claim 4, the cited portion of Barris, in addition to the one described above, does not "compare[e] the emulated image of the subject processor against the native image" but rather describes comparing either a "free [library] core" or the "execution of ...another, trusted, CPU emulator (p. 62,lines 1-27).

With respect to claim 10, the GetContext() function of Barris does not switch between an emulation context and a native context but rather is employed for "context switching in multi CPU machines" (p. 43, lines 20-21), i.e. switching between different CPUs.

With respect to claim 13, the only reference to what might be construed as "two or more verification modes" in the cited section (p. 19, §2.2) is a reference to "two ways of **translating the code** and Applicants submit that "translating code" is not synonymous with verification of code.

With respect to claim 17, the FOA does not provide any specific references to the language of the claims, merely citing the "Testing the Emulator" sections described above. Applicants would appreciate some guidance as to which specific elements of Barris correlate to the specific elements of claim 17. As written, the rejection of claim 17 appears to be an impermissible blanket rejection.

With respect to claim 19, although Barris mentions "indexed or indirect jumps," the examples (Fig. 13, p. 34) do not employ jumps in a manner described by the Applicants' claimed subject matter. Rather, Barris only employs jumps to move around within the emulator and not within the emulated code.

In addition, claims 2-7, 9-14 and 16-20 are allowable because each depends upon an allowable independent claim. Therefore, Applicant respectfully requests withdrawal of the §102(e) rejections of claims 1-3, 5-10, 12-17 and 19-20.

To establish anticipation of a claimed invention under §103(b), all the claim limitations must be taught or suggested by the prior art. (M.P.E.P., §2143.03, citing *in re Royka*, 490 F.2d 981; 180 U.S.P.Q. 580 (CCPA 1974)). In addition, "**All words in a claim must be considered** in judging the patentability of that claim against prior art." (*Id.*, citing *In re Wilson*, 424 F.2d 1382, 1385; 165 U.S.P.Q. 494, 496 (CCPA 1970); *emphasis added*). Applicants believe that the cited art fails to meet this standard. For the reasons above, claims 1, 3-7, 10, 11, 13-19 and 100-111 are allowable over the cited art. In addition to the reasons stated above, claims 3-7, 10, 11, 13-19, 101-105 and 107-111 are allowable because they each depend upon one of the allowable independent claims. Therefore, Applicants respectfully request withdrawal of the §102(b) rejections of claims 1, 3-7, 10, 11, 13-19.

CONCLUSION

In light of the amendments and remarks made herein, Applicants submit that all pending claims are allowable and earnestly solicits notice thereof. Applicants are not conceding in this application that the unamended claims are not patentable over the art cited by the Examiner, as the present claim amendments are only for facilitating expeditious prosecution of the allowable subject matter. Applicants respectfully reserve the right to pursue these and other claims in one or more continuation and/or divisional patent applications. A Request for a Two-Month Extension of Time to file this Amendment and Request for Continued Examination by July 6, 2009 is being filed and paid for concurrently with this filing. It is believed that no other fees are due with the filing of this Amendment/Response. However, should any other fees be due, the Commissioner is hereby authorized to charge such fees to the deposit account of IBM Corporation, Deposit Account No. 09-0447.

Respectfully submitted,

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